



EFM8BB3 USB Type-C 60 W Charger

Board Function

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Revision History

Rev. Description

A00 Prototype version.

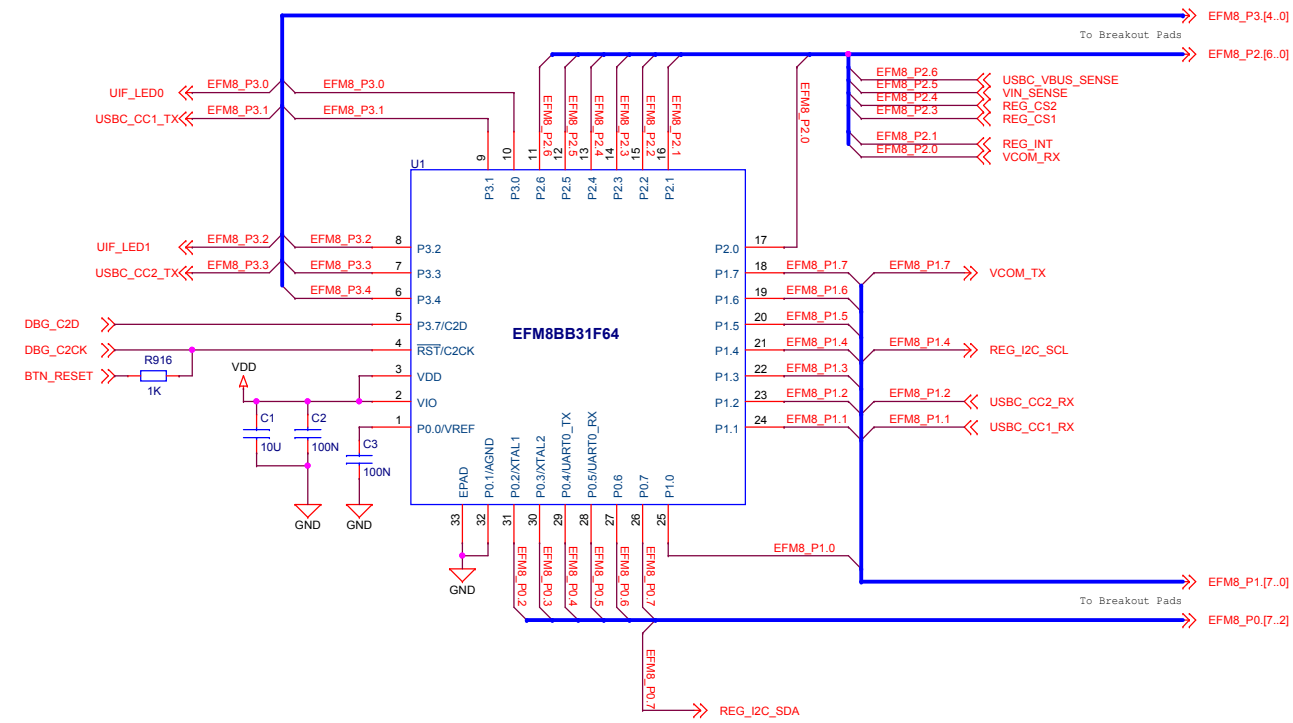
A01 Initial release version.

A02 Disconnected NCP81239 EN from EFM8 to avoid regulator being enabled before firmware starts up.

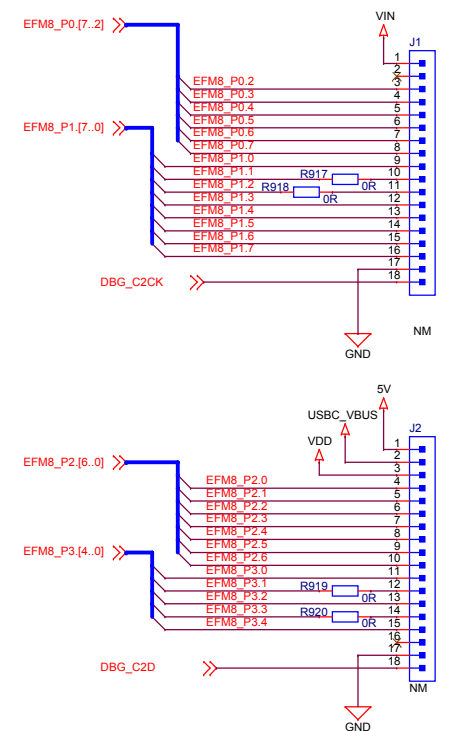


SCHEMATIC1

SILICON LABS		Schematic Title	
EFM8BB3 USB Type-C 60 W Charger		Page Title	
Title Page		Revision	
Document number		A02	
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Monday, April 02, 2012		Tuesday, November 07, 2017	
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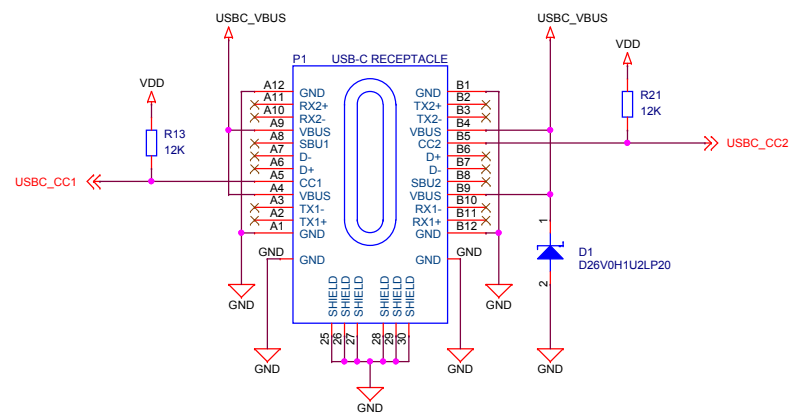


Breakout Pads

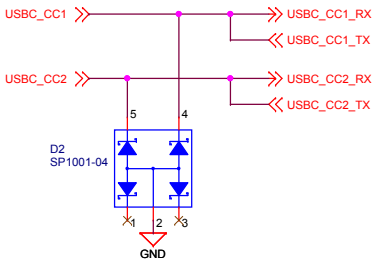


Opt. use R916-R919 series resistors to separate CC1X/RX from break-out pads in case of signal integrity issues.

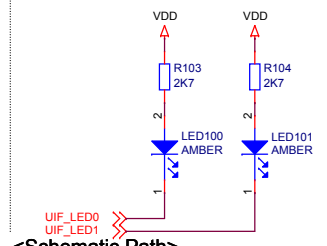
USB TYPE-C Connector and Rp Resistors



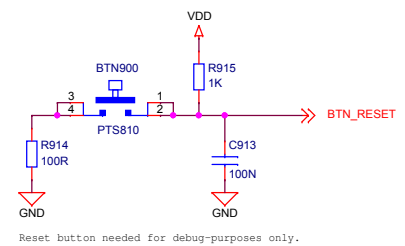
ESD Protection Diodes




LEDs



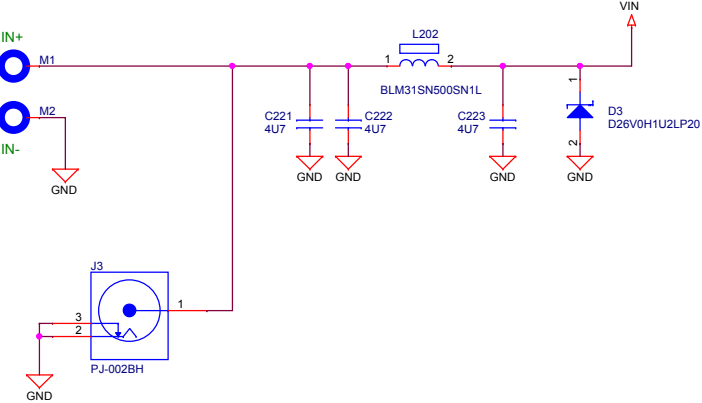
Reset Button



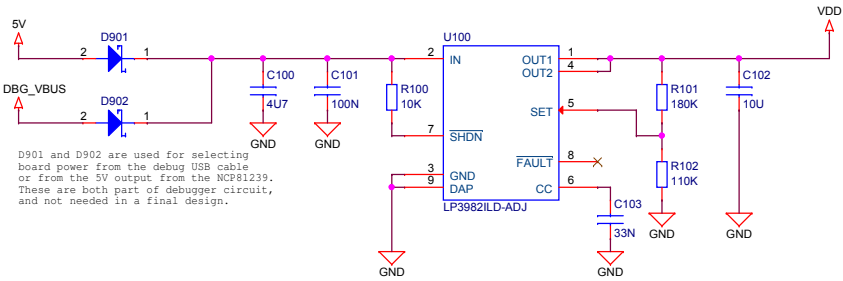
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Designed: JSH		Page Title EFM8BB3 & User Interface	
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Input Voltage Connectors




VDD Regulator



D901 and D902 are used for selecting board power from the debug USB cable or from the 5V output from the NCP81239. These are both part of debugger circuit, and not needed in a final design.

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SCHEMATIC1

 SILICON LABS		Schematic Title	
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U9000
EFM32GG330F1024

DBGMCU_RESET

DBG_VBUS

DBG_3V3

USB_VBUS

USB_VREGI

USB_VREGO

VDD_DREG

AVDD_0

AVDD_1

IOVDD_0

IOVDD_3

IOVDD_5

VSS_PAD

VDD

GND

C901

C902

C903

C904

C905

C906

C907

C908

C909

L901

CIM03U241

1

2

20

52

45

46

39

8

26

55

65

27

23

100N

1U

100N

100N

100N

1U

10N

4U7

SPI Flash

The diagram shows the connection of two SPI Flash chips, U902A and U902B, to the DBGMCU. U902A is an MX25R8035F chip with pins D2 (SI / SIO0), E1 (SO / SIO1), A3 (CS#), E3 (WP# / SIO2), and C1 (RESET# / SIO3). It is connected to DBGMCU_SPI_MOSI, DBGMCU_SPI_SCLK, and DBGMCU_SPI_CS. U902B is also an MX25R8035F chip with pins VCC (A1) and GND (B2). It is connected to DBGMCU_SPI_CS and GND. A 330K resistor R907 is connected between DBGMCU_SPI_CS and DBGMCU_SPI_MOSI. A 100N capacitor C911 is connected between VCC and GND.

Note: The SPI flash is only available to the debug mcu when the USB cable is plugged in!

Board ID EEPROM

The diagram illustrates the Board ID EEPROM circuit. It features two 24AA024 EEPROMs, U901A and U901B. U901A is connected to the DBG_3V3 supply via resistors R904 (4K7) and R905 (4K7) for the SDA and SCL lines. Its address pins A0, A1, and A2 are connected to GND. Its write protect (WP) pin is connected to the DBG_3V3 supply via resistor R906 (10K) and to the BOARD_ID_WP signal. U901B has its VCC pin connected to the DBG_3V3 supply via capacitor C910 (100nF) and its VSS pin connected to GND. Its data bus (pins 1-4) is connected to the BOARD_ID_SDA and BOARD_ID_SCL signals.

Debug MCU Connections

U900A
EFM32GG330F1024

1 PA0 / GPIO_EM4WU0 / I2C0_SDA #0 / LEU0_RX #4 / PRS_CH0 / TIM0_CC0 #0.1,4
3 PA1 / CMU_CLK1 #0 / I2C0_SCL #0 / PRS_CH1 / TIM0_CC1 #0.1
4 PA2 / CMU_CLK0 #0 / ETM_TD0 #3 / TIM0_CC2 #0.1
5 PA3 / ETM_TD1 #3 / LES_ALTEX2 / TIM0_CDT10 #0
6 PA4 / ETM_TD2 #3 / LES_ALTEX3 / TIM0_CDT11 #0
7 PA5 / ETM_TD3 #3 / LES_ALTEX4 / LEU1_TX #1 / TIM0_CDT12 #0
17 PA6 / ETM_TCLK #3 / GPIO_EM4WU1 / LEU1_RX #1
18 PA8 / TIM2_CC0 #0
19 PA9 / TIM2_CC1 #0
64 PA10 / TIM2_CC2 #0
PA15 / TIM3_CC2
15 PB7 / LFXLTAL_P / TIM1_CC0 #3 / US0_TX #4 / US1_CLK #0
21 PB8 / LFXLTAL_N / TIM1_CC1 #3 / US0_RX #4 / US1_CS #0
22 PB11 / DAC0_OUT0 / OPAMP_OUT0 / I2C1_SDA #1 / LETIMO_OUT0 #1 / TIM1_CC2 #3
24 PB12 / DAC0_OUT1 / OPAMP_OUT1 / I2C1_SCL #1 / LETIMO_OUT1 #1
25 PB13 / HFXLTAL_P / LEU0_TX #1 / US0_CLK #4.5
PB14 / HFXLTAL_N / LEU0_RX #1 / US0_CS #4.5

U900B
EFM32GG330F1024

9 PC0 / ACMP0_CH0 / DAC0_OUTALT / OPAMP_OUT0ALT #1 / I2C0_SDA #4 / LES_CH0 / PCNT0_S0IN #2 / PRS_CH2 #0 / TIM0_CC1 #4 / US0_TX #5 / US1_TX #0
10 PC1 / ACMP0_CH1 / DAC0_OUTALT / OPAMP_OUT0ALT #1 / I2C0_SCL #4 / LES_CH1 / PCNT0_S1IN #2 / PRS_CH3 #0 / TIM0_CC2 #4 / US0_RX #5 / US1_RX #0
11 PC2 / ACMP0_CH2 / DAC0_OUTALT / OPAMP_OUT0ALT #2 / LES_CH2 / TIM0_CDT10 #4 / US2_TX
12 PC3 / ACMP0_CH3 / DAC0_OUTALT / OPAMP_OUT0ALT #3 / LES_CH3 / TIM0_CDT11 #4 / US2_RX
13 PC4 / ACMP0_CH4 / DAC0_P0 / OPAMP_P0 / I2C1_SDA #0 / LES_CH4 / LETIMO_OUT0 #3 / PCNT1_S0IN / TIM0_CDT12 #4 / US2_CLK
14 PC5 / ACMP0_CH5 / DAC0_N0 / OPAMP_N0 / I2C1_SCL #0 / LES_CH5 / LETIMO_OUT1 #3 / PCNT1_S1IN / US2_CS
37 PC6 / ACMP0_CH6 / ETM_TCLK #2 / I2C0_SDA #2 / LES_CH6 / LEU1_TX #0
38 PC7 / ACMP0_CH7 / ETM_TD0 #2 / I2C0_SCL #2 / LES_CH7 / LEU1_RX #0
41 PC8 / ACMP1_CH0 / LES_CH8 / TIM2_CC0 #2 / US0_CS #2
42 PC9 / ACMP1_CH1 / GPIO_EM4WU2 / LES_CH9 / TIM2_CC1 #2 / US0_CLK #2
43 PC8 / ACMP1_CH2 / LES_CH10 / TIM2_CC2 #2 / US0_RX #2
44 PC11 / ACMP1_CH3 / LES_CH11 / US0_TX #2
28 PD0 / ADC0_CH0 / DAC0_OUTALT / OPAMP_OUT0ALT #4 / DAC0_OUT2 / OPAMP_OUT2 #1 / PCNT2_S0IN #0 / US1_TX #1
29 PD1 / ADC0_CH1 / DAC0_OUT1ALT / OPAMP_OUT1ALT #4 / DBG_SWO #2 / PCNT2_S1IN #0 / TIM0_CC0 #3 / US1_RX #1
30 PD2 / ADC0_CH2 / DBG_SWO #3 / TIM0_CC1 #3 / US1_CLK #1 / USB_DMPU
31 PD3 / ADC0_CH3 / DAC0_N2 / OPAMP_N2 / ETM_TD1 #0.2 / TIM0_CC2 #3 / US1_CS #1
32 PD4 / ADC0_CH4 / DAC0_P2 / OPAMP_P2 / ETM_TD2 #0.2 / LEU0_TX #0
33 PD5 / ADC0_CH5 / DAC0_OUT2 / OPAMP_OUT2 #0 / ETM_TD3 #0.2 / LEU0_RX #0
34 PD6 / ACMP0_O #2 / ADC0_CH6 / DAC0_P1 / OPAMP_P1 / ETM_TD0 #0 / I2C0_SDA #1 / LES_ALTEX0 / LETIMO_OUT0 #0 / PCNT0_S0IN #3 / TIM1_CC0 #4 / US1_RX #2
35 PD7 / ACMP1_O #2 / ADC0_CH7 / CMU_CLK0 #2 / DAC0_N1 / OPAMP_N1 / ETM_TCLK #0 / I2C0_SCL #1 / LES_ALTEX1 / LETIMO_OUT1 #0 / PCNT0_S1IN #3 / TIM1_CC1 #4 / US1_TX #1
36 PD8 / BU_VIN / CMU_CLK1 #1

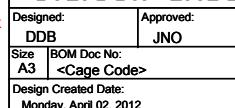
U900C
EFM32GG330F1024

56 PE8 / PCNT2_S0IN #1 / PRS_CH3 #1
57 PE9 / PCNT2_S1IN #1
58 PE10 / BOOTLOADER_TX / TIM1_CC0 #1 / US0_TX #0
59 PE11 / BOOTLOADER_RX / LES_ALTEX5 / TIM1_CC1 #1 / US0_RX #0
60 PE12 / CMU_CLK1 #2 / I2C0_SDA #6 / LES_ALTEX6 / TIM1_CC2 #1 / US0_CLK #0 / US0_RX #3
61 PE13 / ACMP0_O #0 / GPIO_EM4WU5 / I2C0_SCL #6 / LES_ALTEX7 / US0_CS #0 / US0_TX #3
62 PE14 / LEU0_TX #2 / TIM3_CC0
63 PE15 / LEU0_RX #2 / TIM3_CC1
49 PF0 / DBG_SWCLK #0.1,2,3 / I2C0_SDA #5 / LETIMO_OUT0 #2 / LEU0_TX #3 / TIM0_CC0 #5 / US1_CLK #2
50 PF1 / DBG_SWIO #0.1,2,3 / GPIO_EM4WU3 / I2C0_SCL #5 / LETIMO_OUT1 #2 / LEU0_RX #3 / TIM0_CC1 #5 / US1_CS #2
51 PF2 / ACMP1_O #0 / DBG_SWO #0 / GPIO_EM4WU4 / LEU0_TX #4 / TIM0_CC2 #5
52 PF5 / PRS_CH2 #1 / TIM0_CDT12 #2.5 / USB_VBUSEN
47 PF10 / USB_DM
48 PF11 / USB_DP
53 PF12 / USB_ID

TP900
Bootloader Halt pin

<Schematic Path>
SCHEMATIC1

Debug MCU SWD Header

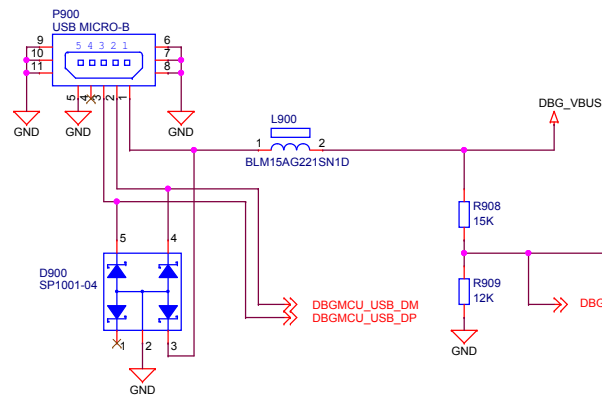


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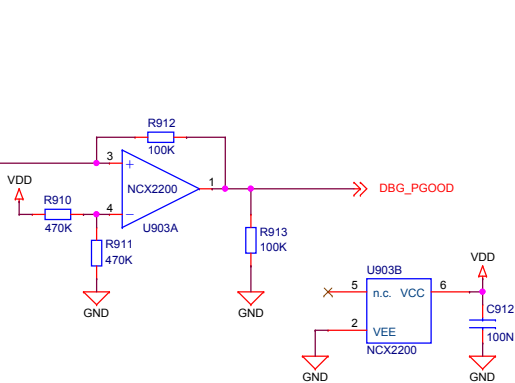
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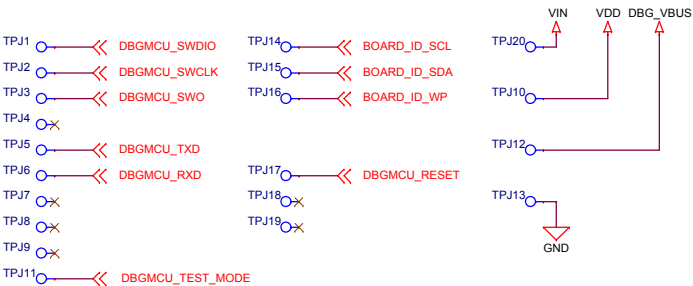
Debug USB Connector




Debug USB Cable Detect



Test Points



<Schematic Path>
SCHEMATIC1

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